AMENDMENTS TO THE SPECIFICATION

Please amend the title of the application to read as follows:

SUBSTRATE FOR GROWTH OF NITRIDE SEMICONDUCTOR ~~GROWTH~~

Paragraph [0006], page 2, line 20, replace the paragraph with the following:

The first is a growth method of GaN using a low-temperature AlN buffer layer (see the following Non-Patent Document 1). This method is as follows. The sapphire substrate was heated up to the temperature around 1000 °C for surface cleaning in metalorganic vapor phase epitaxy system etc., the temperature was then once dropped. Next, a low-temperature ~~AlN~~ AlN buffer layer was deposited at around 500 °C, and the temperature is again raised. Then, GaN was grown at around 1000 °C . The AlN buffer layer deposited by this method is amorphous and the islands were formed during the temperature rising step due to the solid phase growth of amorphous ~~AlN~~ AlN. As a matter of course, the island shape to be formed varies depending upon the atmosphere in the growth system (apparatus)or the temperature rising rate during the temperature rising. At the beginning of growth of the ~~AlN buffer~~ GaN layer at high temperatures, this island becomes a nucleus, whereby the ~~AlN buffer~~ GaN layer undergoes crystal growth. During that crystal growth, flattening of the ~~AlN buffer~~ GaN layer advances due to the coalescence. GaN undergoes two-dimensional crystal growth on the flattened ~~GaN buffer~~ GaN layer.

Paragraph [0009], page 4, line 1, replace the paragraph with the following:

As described previously, in all of these growth methods, the buffer layer was aimed to achieve lattice matching with the GaN layer, but lattice matching with the substrate was not taken into consideration.

Also, even if the buffer layer is deposited at a low temperature, the low-temperature buffer layer is amorphous and solid phase growth occurs at the time of temperature rising. For that reason, the lattice mismatch between the buffer layer and the substrate still exists, it is difficult to effectively suppress the generation of ~~transition~~ crystal defects, and threading dislocation of 10^9 to 10^{10} cm^{-2} exists usually. It is well known that this dislocation deteriorates the characteristics of a fabricated device. For example, shortening of the life of laser and an increase of leak current and a lowering of breakdown voltage of the device. Also, diffusion or segregation of impurities may possibly be promoted due to the existence of the dislocation. Accordingly, reducing the dislocation density in the nitride semiconductor layer is very important for improving the device characteristics, realizing devices which have not been attained so far due to influences of the dislocation and enhancing the controllability in fabrication of a device structure in crystal growth.

Paragraph [0011], page 4, line 28, replace the paragraph with the following:

Non-Patent Document 1:

H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, "Meta illustrated in the foregoing embodiment, the GaN buffer layer 9 (thickness: 1 μm), the n^+-type GaN subcollector layer 10 (thickness: 1 μm), the n^--type GaN collector layer 11 (thickness: 0.5 μm), the p-type GaN base layer 12 (thickness: 0.08 μm), the n^--type $Al_{1-x}Ga_xN$ emitter layer 13 ($0 \leq x < 1$) (thickness: 0.05 μm), and the n^+-type GaN contact layer 14 (thickness: 0.1 μm) were grown by the metalorganic vapor phase epitaxy. In this case, the growth sequence is a method in which the substrate 6 for growth of nitride semiconductor was introduced into a growth furnace, the temperature was then raised to the growth temperature (1,000 °C) under an ammonia atmosphere, and a source material gas was supplied. Trimethylgallium, trimethylaluminum and ammonia are used as the source materials. For dopant of

n-type impurities, a ~~silane~~ Si was used. For dopant of p-type impurities, Mg was used. A mesa structure was prepared by etching, and ohmic electrodes, i.e., the collector electrode 15, the base electrode 16, and the emitter electrode 17, were formed on the each exposed layers by means of electron beam metal deposition. In a collector current-collector voltage characteristic in common emitter configuration of a ~~fabricatied~~ fabricated transistor, current gain of approximately 100 was obtained, and the breakdown voltage was increased to approximately 200 V with a reduction of the dislocation density as described already being reflected.